

UMA (11.6")

Intel Brasswell-M Platform Block Diagram

Charger	PG.30
+3VS5/+5VS5	PG.31
DDR3L	PG.32
MOIC	PG.33
CPU Core	PG.34,35

DDR3L	1600MT/s
Memory down*4pcs	Channel A
PG.14	
DDR3L	1600MT/s
Memory down*4pcs	Channel B
PG.15	

Intel Brasswell

Power : 4.5 (Watt)

Package : BGA1170

Size : 25 X 27 (mm)

eDP (2 lane)

EDP to LVDS

PG.16

LCD connector

PG.17

DP Port0

HDMI

PG.18

eMMC 4.51

eMMC
32G/64G
/128GB

PG.24

PCI-E x2

Card Reader
RTS5239-GR

PG.21

WLAN
BT COMBO
NGFF M2

PG.27

PG.2~13

USB 3.0

USB 2.0

USB 2.0

Touch
Screen

PG.17

Webcam

PG.18

USB3.0 Ports
X1

PG.25

USB2.0 Ports
X1

PG.24

USB 2.0

USB 2.0 Hub

PG.26

USB2.0 Port
X1

PG.24

WLAN
BT COMBO
NGFF M2

PG.27

WWAN(Optional)
NGFF M2

PG.24

KBC
IT8987

PG.28

LPC

Fast SPI

KB

PG.23

TP

PG.23

ROM

PG.28

AUDIO
CODEC
ALC 3227

PG.19

Speaker

PG.19

Azalia

Hp

Combo Jack

PG.20

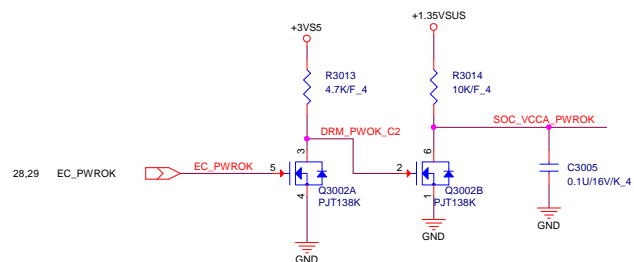
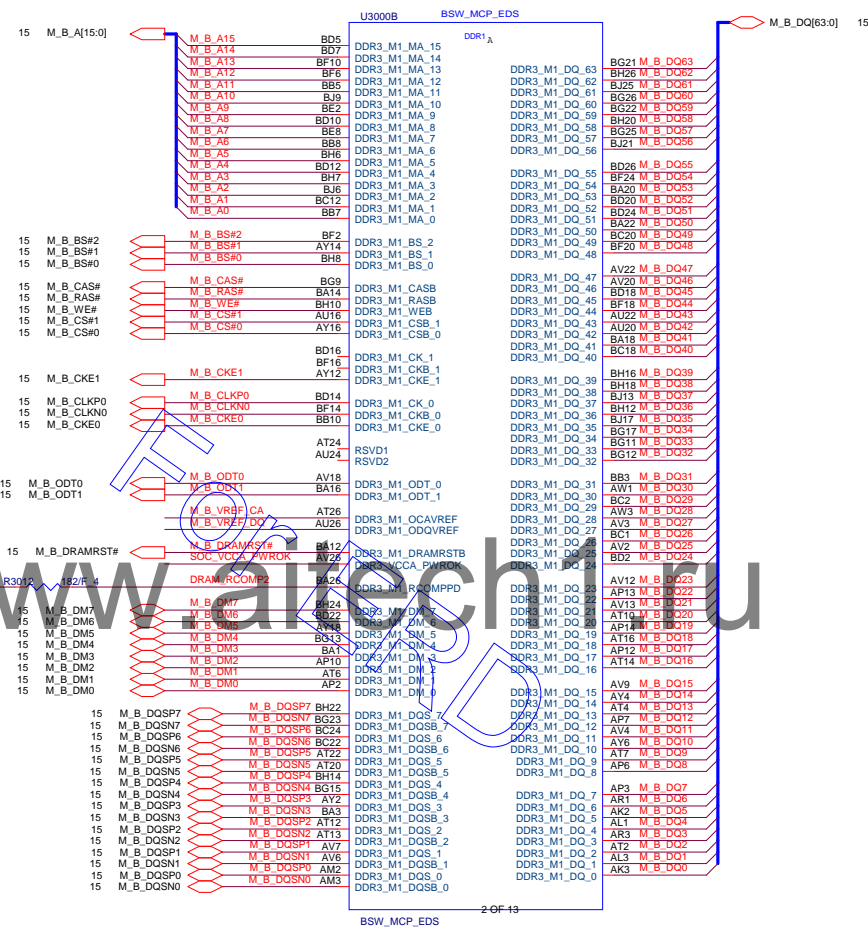
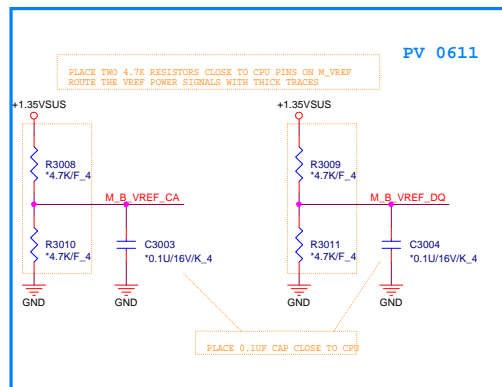
MIC

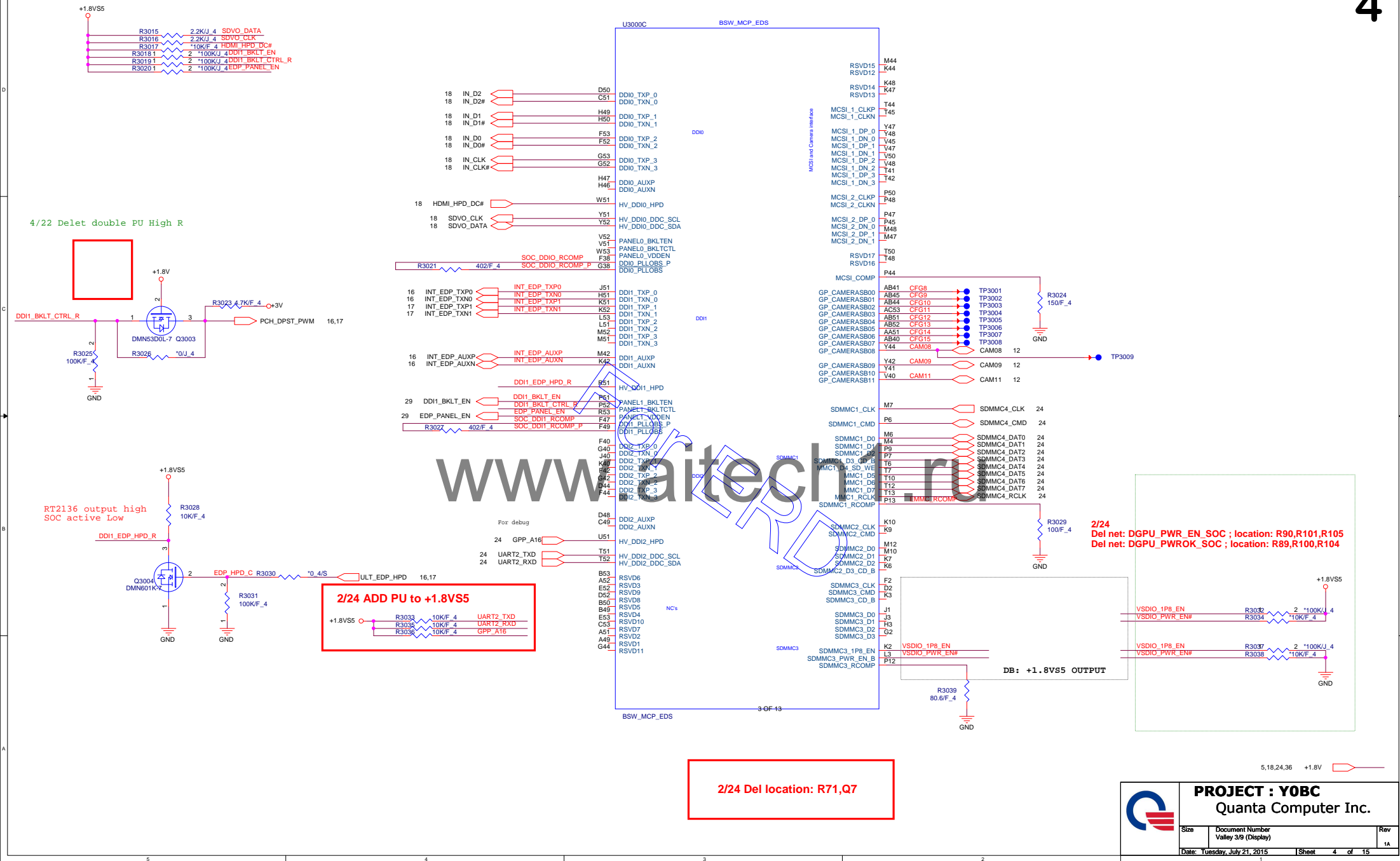


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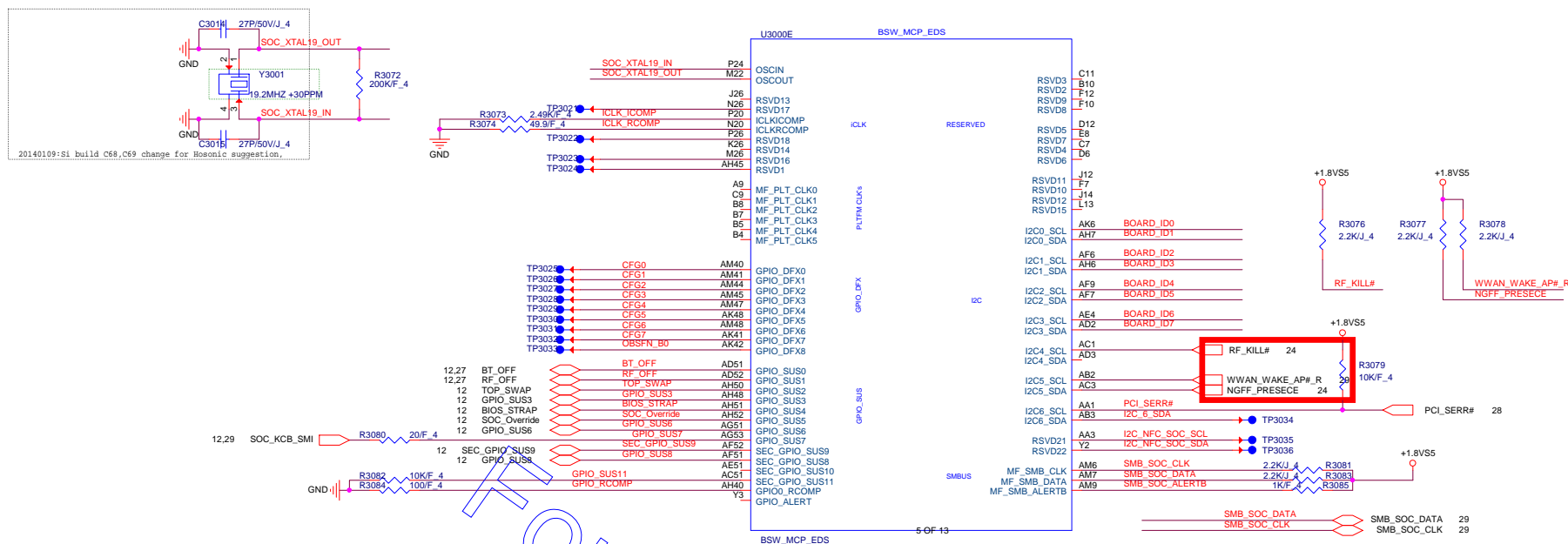
Size	Document Number	Rev
	BLOCK DIAGRAM	1A
Date: Tuesday, July 21, 2015	Sheet	1 of 15







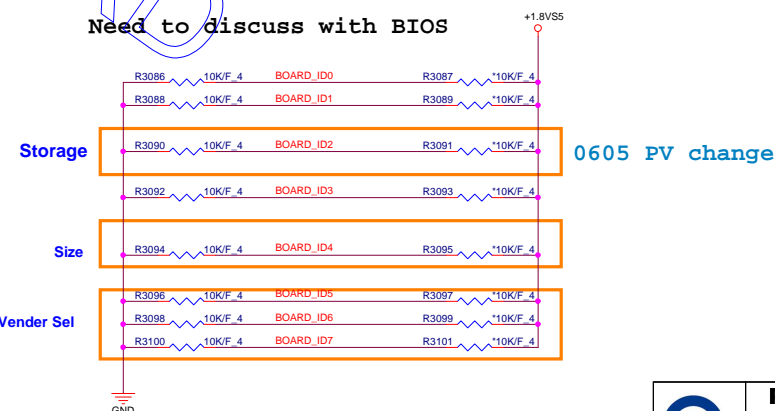


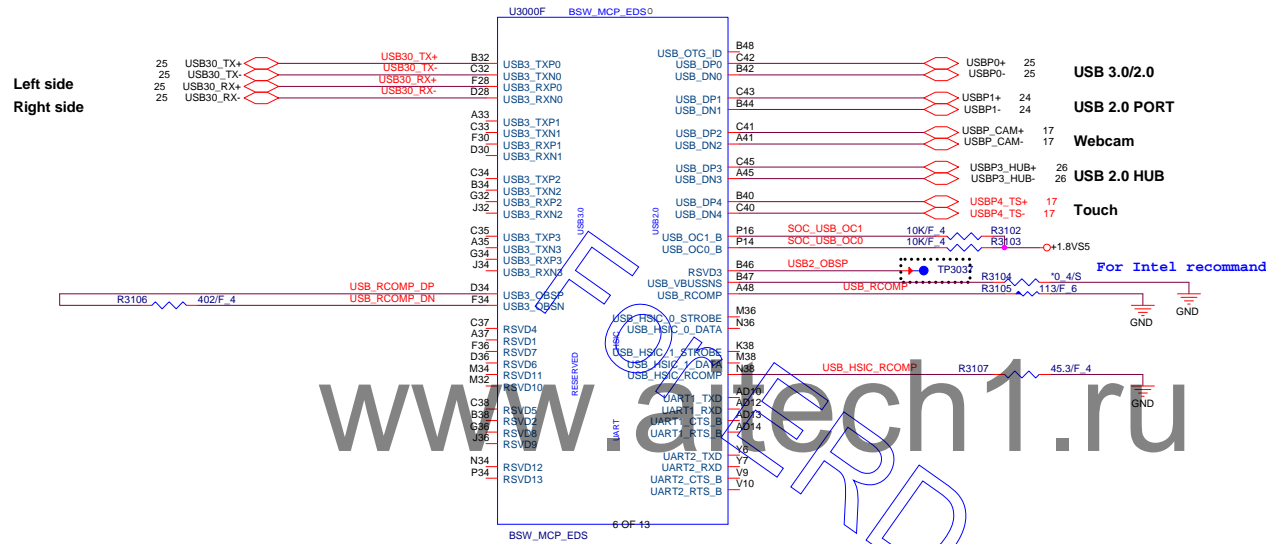


BOARD ID SETTING

	Reserve (Default = 000)			Size		Storage	EMMC	Reserved
Model	BOARD_ID7	BOARD_ID6	BOARD_ID5	BOARD_ID4	BOARD_ID3	BOARD_ID2	BOARD_ID1	BOARD_ID0
Samsung	0	1	0	2G=0	0	0 : emmc	0 : 32G	0
Mircon	0	0	1	4G=1	0	1 : HDD	1 : 64G	0
Hynix	0	0	0	0	0			0

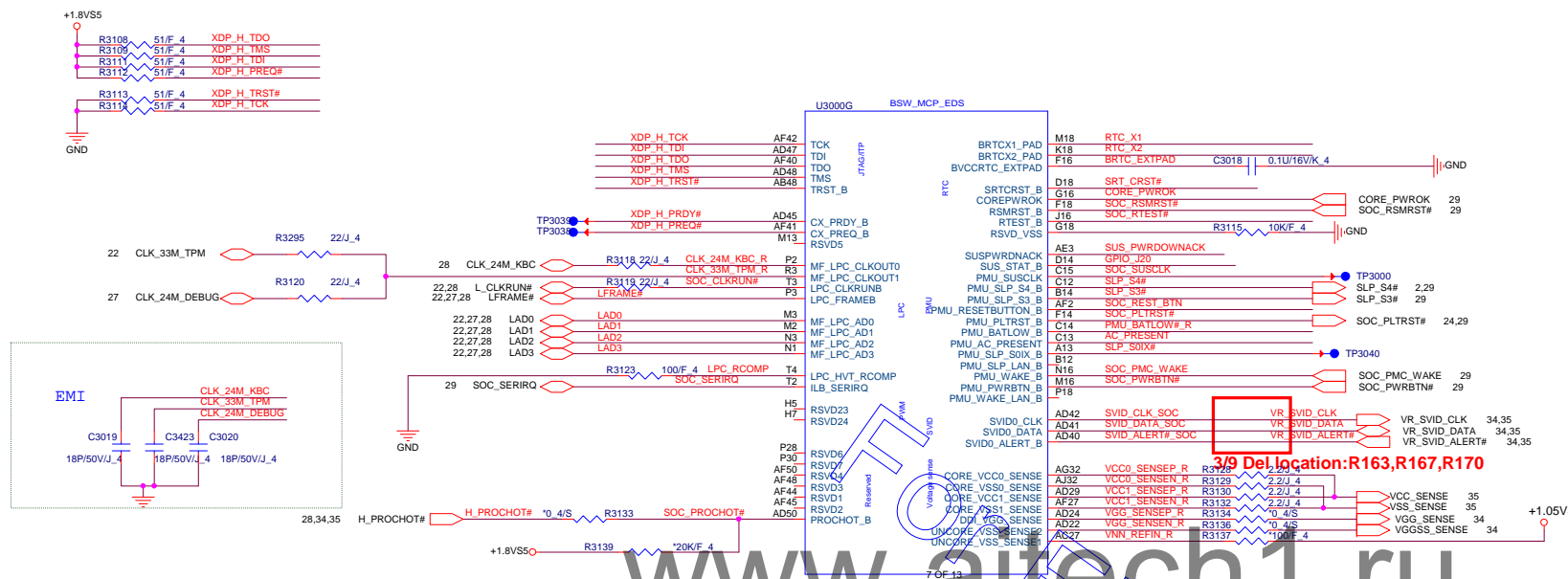
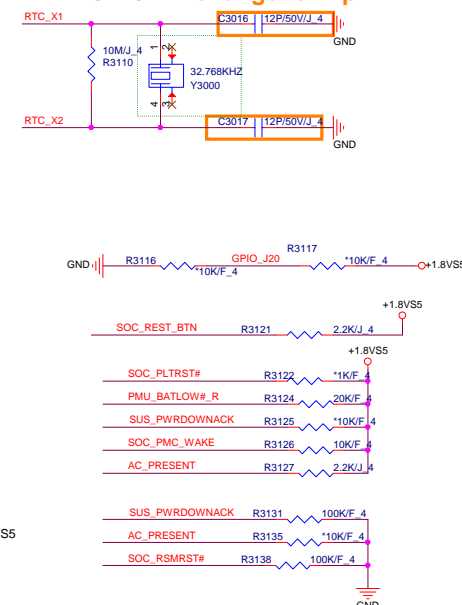
Need to discuss with BIOS





RTC Clock 32.768KHz

0716 MV change to 12p



3/3 Del net: VR_SVID_ALERT#/VR_SVID_DATA/VR_SVID_CLK; location: R166,R42,R43,R16,R20

Close to CPU R111

Close to VCC power control PU11

Close to VGG power control PU10

RTC Circuitry(RTC)

DTG Powertraps with 20mils

Del RTC net: +BAT_RTC

0

3V_RTC_0 R3143 1K/F_4 +3V_RTC_1

D300
BAT54CW-7-F

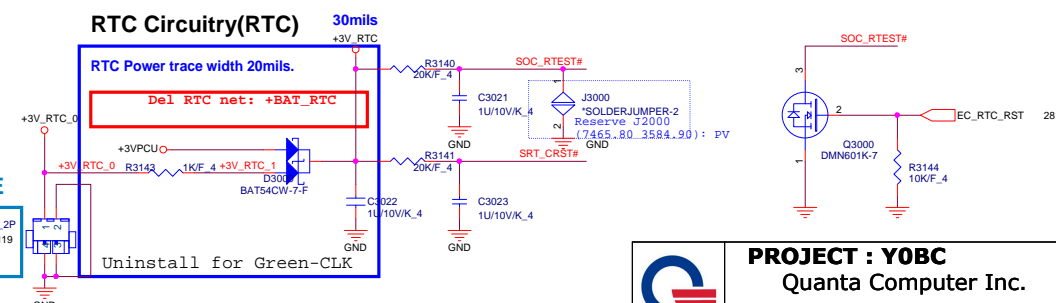
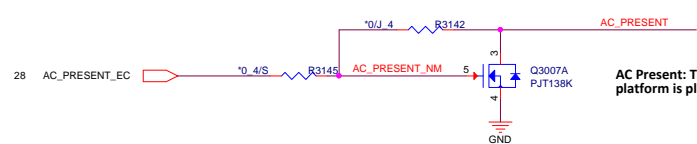
Uninstall for Green-CLK^{GND}

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PV 0601 CHANGE

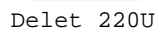
CN3000
RTC_CONN_2P
DFHD02MS119

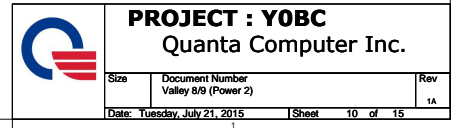
AC Present: This input pin indicates when the platform is plugged into AC power.

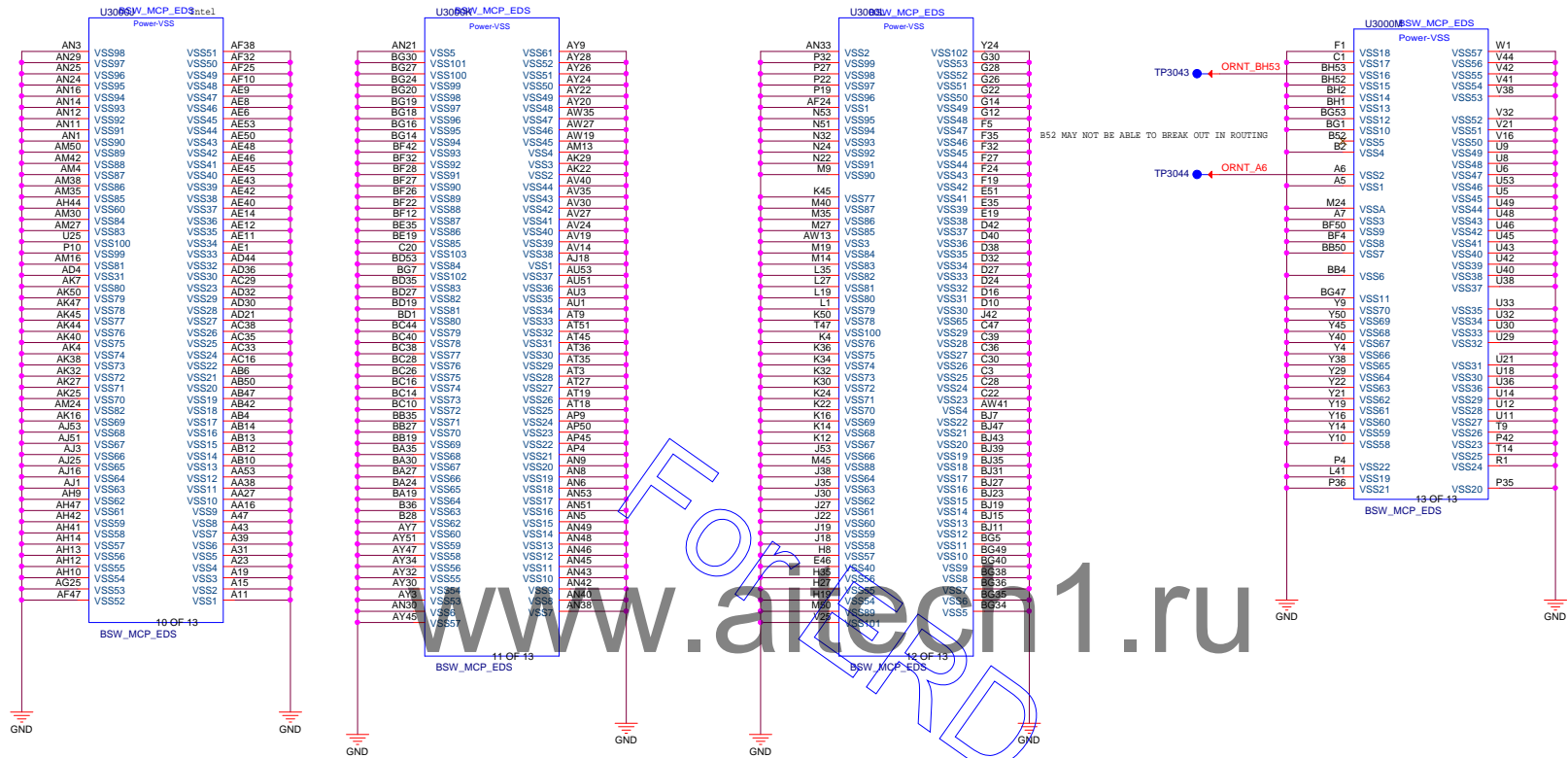


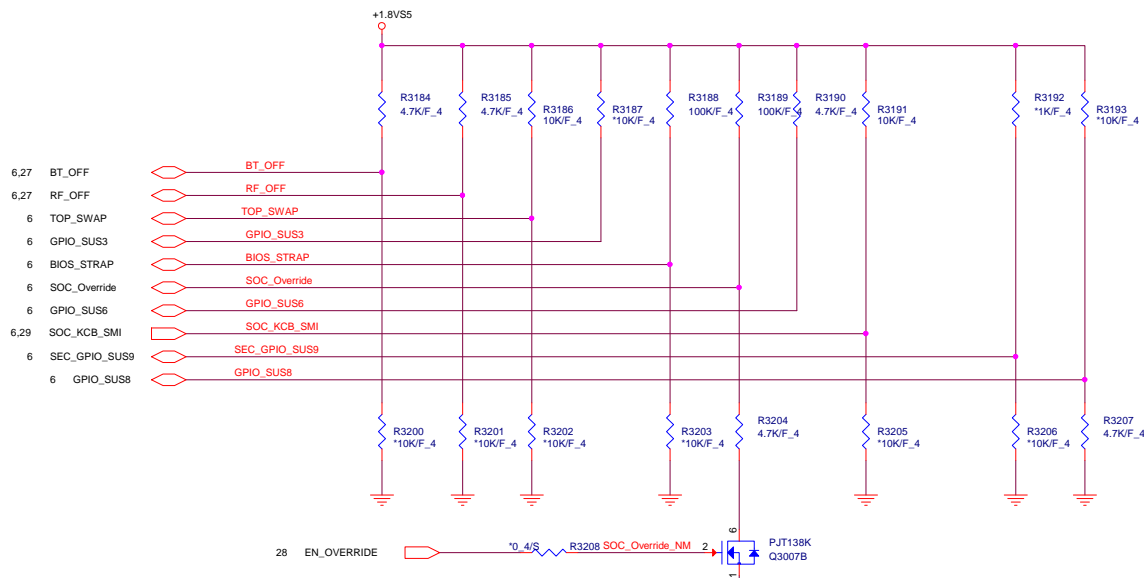
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Size	Document Number Valley 6/9 (USB/LPC/I2C)	Rev
Date: Tuesday, July 21, 2015	Sheet 8 of 15	1A

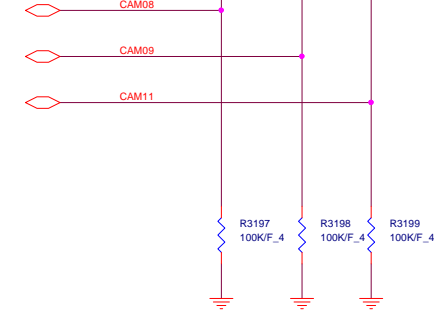








4 CAM08
4 CAM09
4 CAM11



REQUIRED STRAPS

	GPIO_SUS0	GPIO_SUS1	TOP_SWAP	GPIO_SUS3	BIOS_STRAP	SOC_Override	GPIO_SUS6	SOC_KCB_SMI	GPIO_SUS8
PULL HIGH	DDI0 detected DEFAULT	DDI1 detected DEFAULT	Normal Operation DEFAULT	Reserve 10 KΩ PU DEFAULT	SPI DEFAULT	Normal Operation	10 KΩ PU to 1.8V DEFAULT	Reserve 10 KΩ PU DEFAULT	Supply is 1.35V
PULL LOW	DDI0 not detected	DDI1 not detected	Change Boot Loader address		LPC	Override DEFAULT			Supply is 1.25V DEFAULT

	CAM08	CAM09	CAM11
PULL HIGH	ICLK Xtal OSC Bypass	CCU SUS RO Bypass	RTC OSC Bypass
PULL LOW	ICLK Xtal OSC No Bypass DEFAULT	CCU SUS RO No Bypass DEFAULT	RTC OSC No Bypass DEFAULT



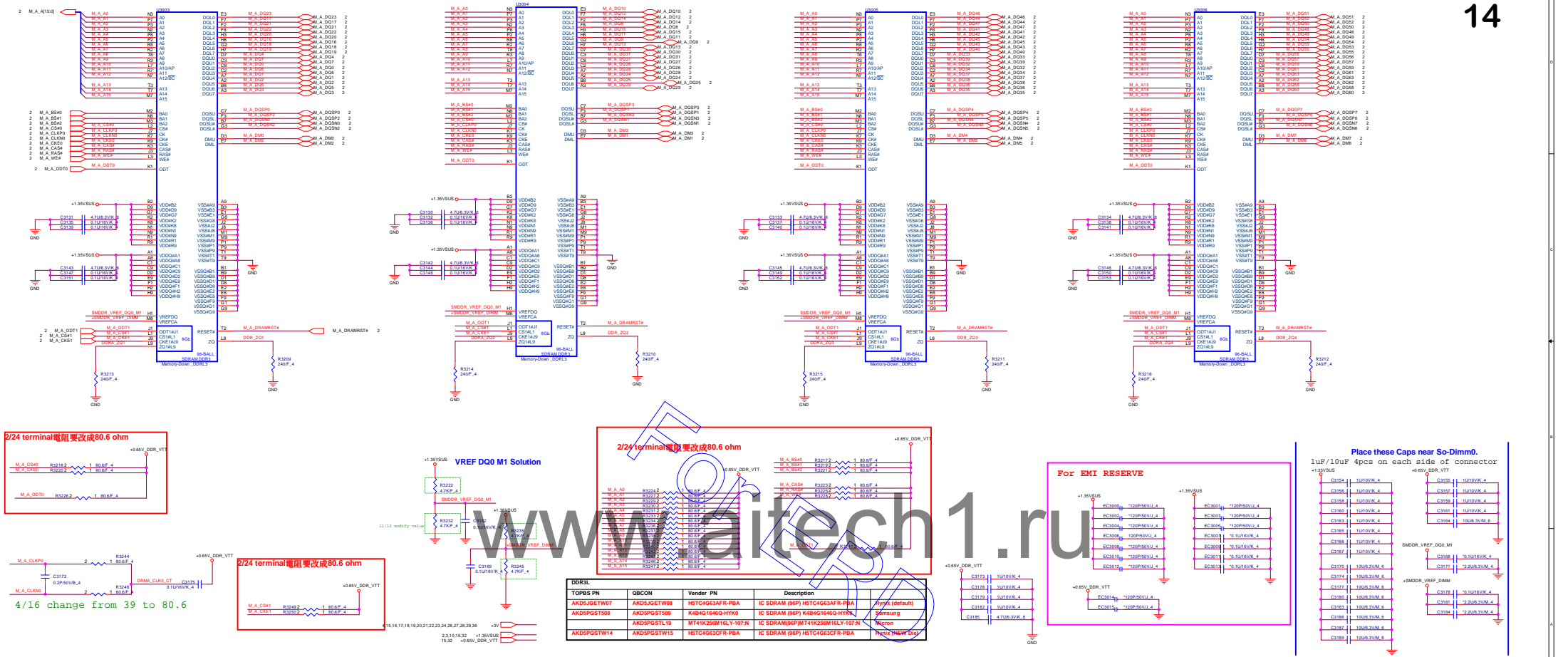
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Size	Document Number	Rev
	Valley 9/9 (GND)	1A
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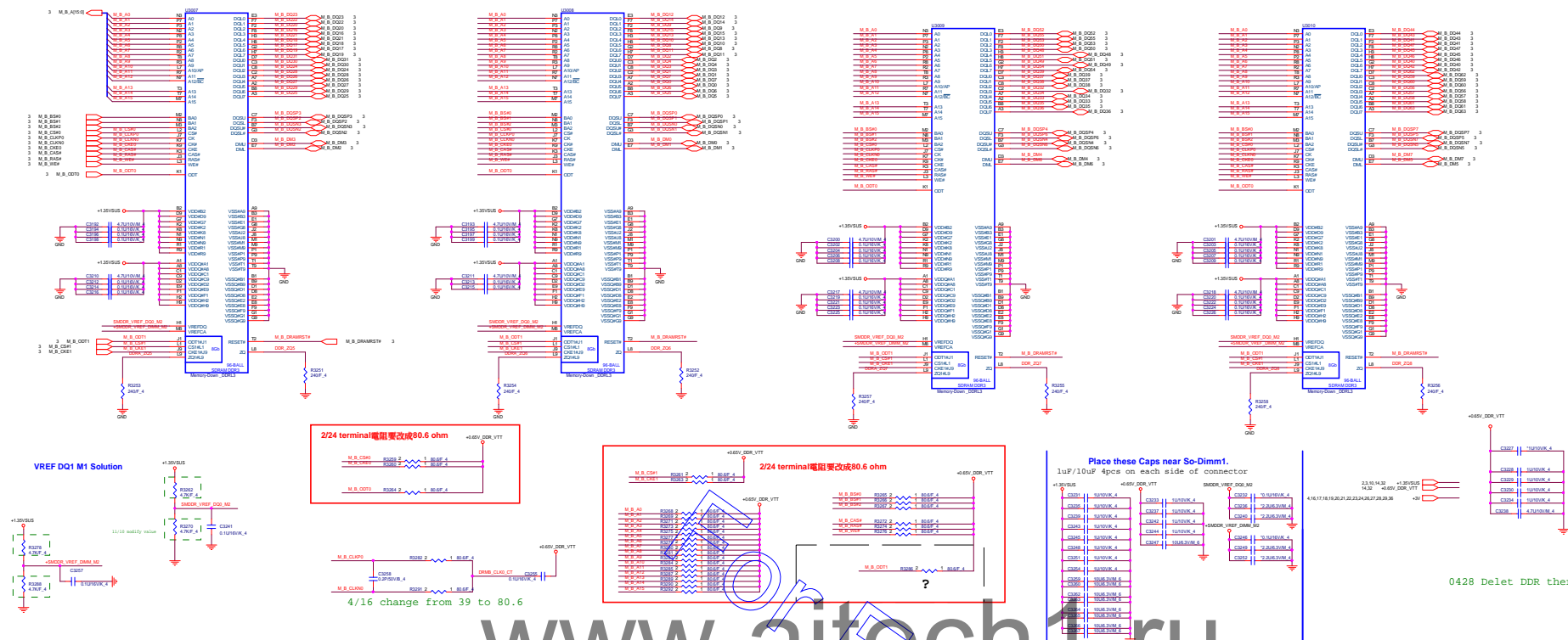
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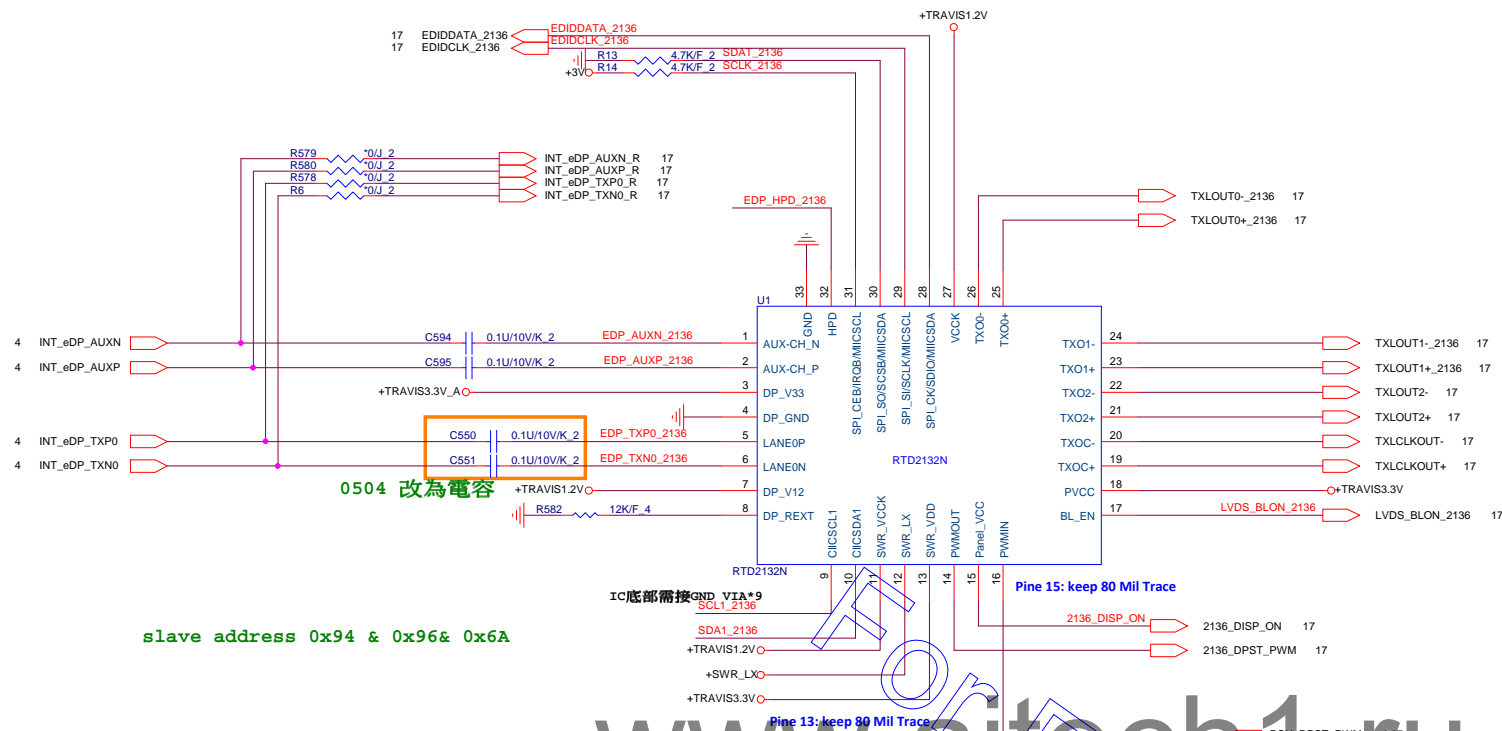
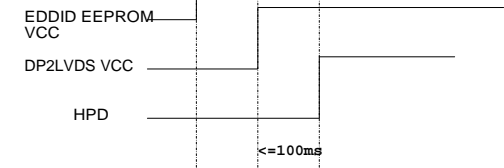
APS <Location : CN5>

FORGERD
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API <Location : D1,D2,Q10,U5,R119,R122,R124,R127,R179,U7>

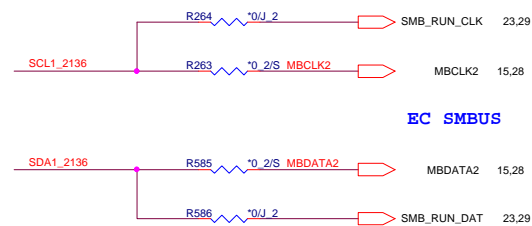
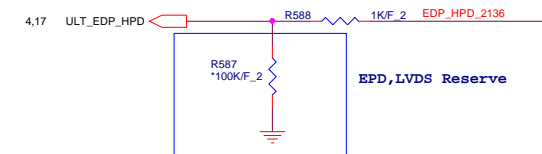


TOPSS PN	QBCON	Vender PN	Description	Pin# (default)
AKDSJGETW07	AKDSJGETW08	HSTC4G3AFR-PBA	IC SDRAM (8P) HSTC4G3AFR-PBA	Pin#A (default)
AKDSPGSTW08	AKDSPGSTW09	K4B4G1646Q-HYK0	IC SDRAM (8P) K4B4G1646Q-HYK0	Pin#A (default)
AKDSPGSTW10	AKDSPGSTW11	MT41K256M16L-Y107-N	IC SDRAM (8P) MT41K256M16L-Y107-N	Pin#A (default)
AKDSPGSTW14	AKDSPGSTW15	HSTC4G3CFR-PBA	IC SDRAM (8P) HSTC4G3CFR-PBA	Pin#A (default)





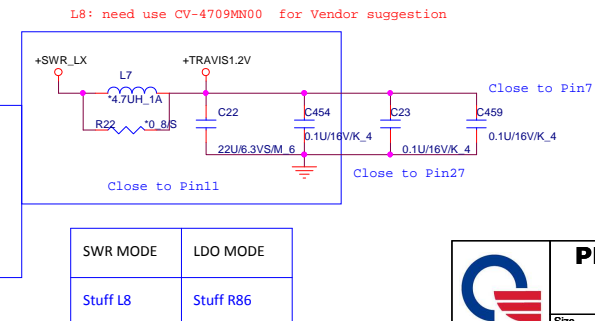
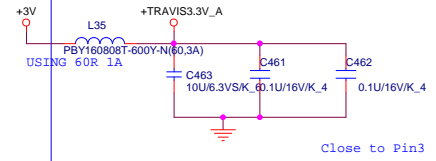
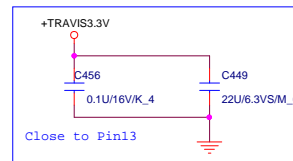
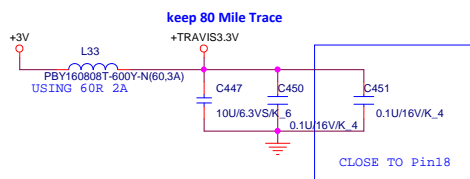
```
slave address 0x94 & 0x96& 0x6A
```



EC SMBUS

Default: ROM ONLY MODE

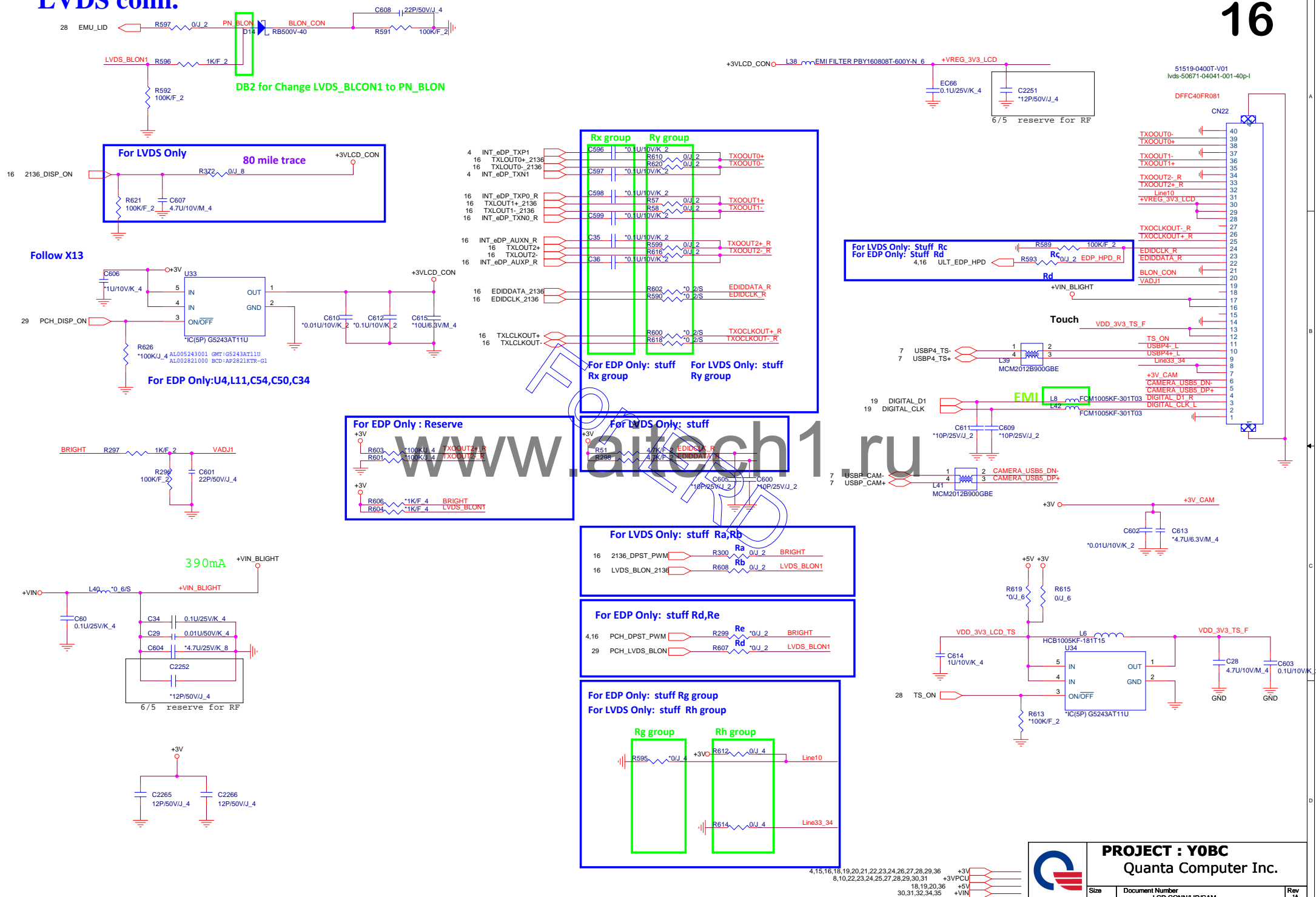
		MODE_CFG0(PIN47)	
		0	1
MODE_CFG1(PIN48)	0	x	EP MODE
	1	ROM ONLY MODE	EEPROM MO

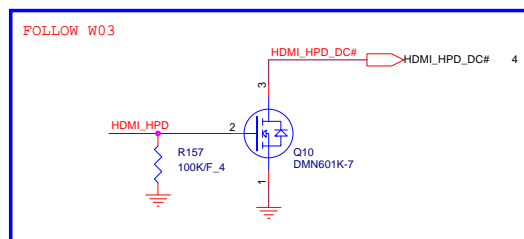


SWR MODE	LDO MODE
Stuff L8	Stuff R86

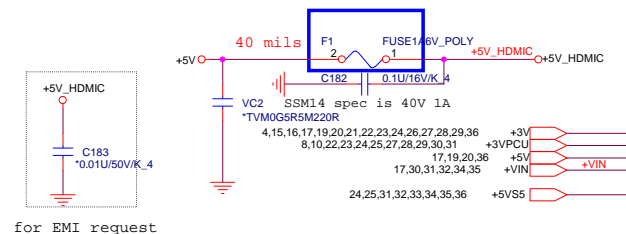


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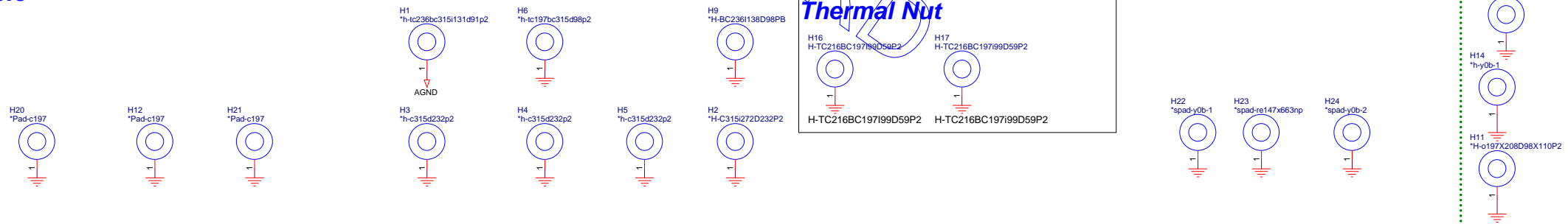
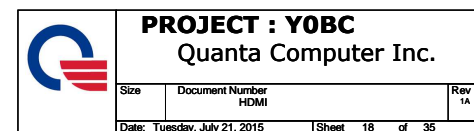


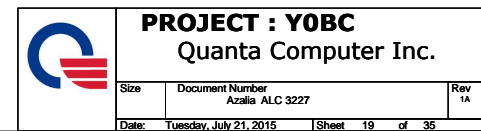


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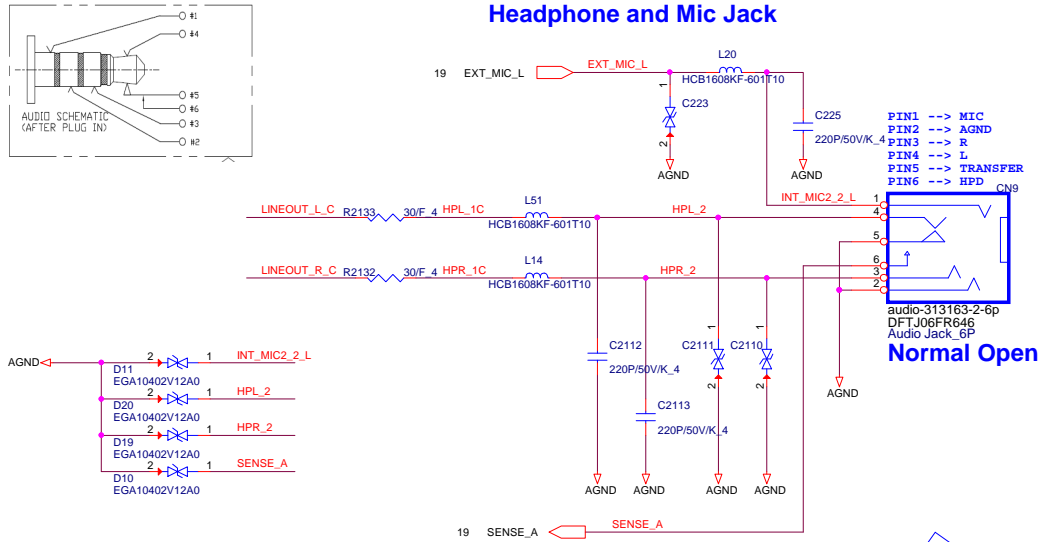
Thermal Nut

**EMI**

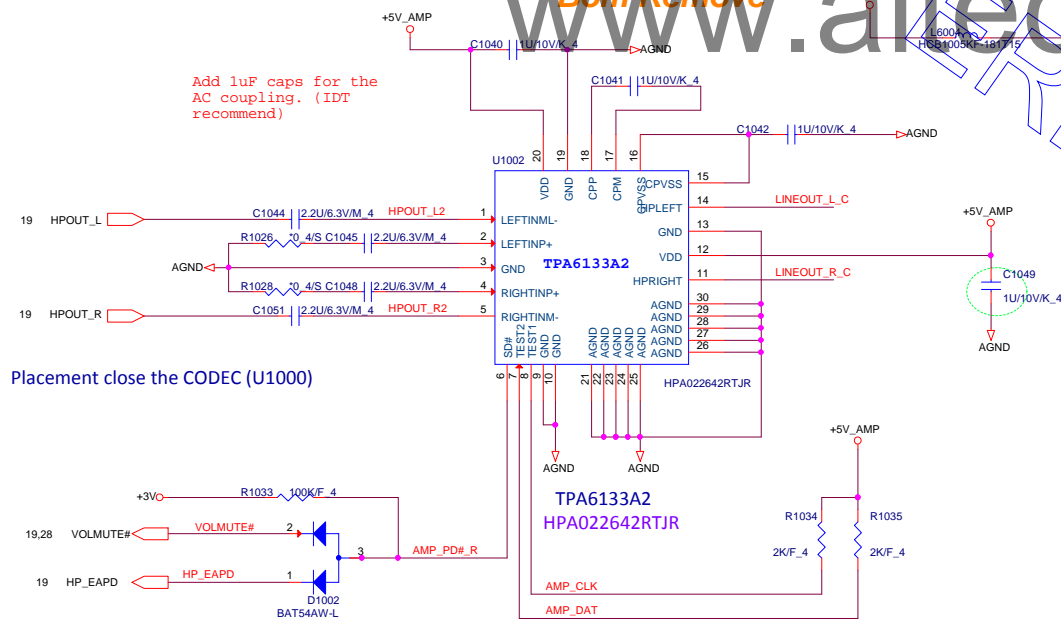


Head Phone out

Headphone and Mic Jack



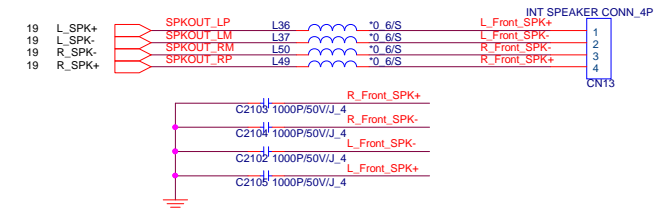
Head Phone out



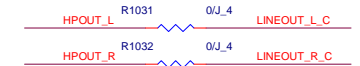
Int. SPEAKER

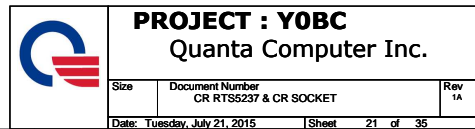
Front Speaker Conn

Front speaker(from Amp)

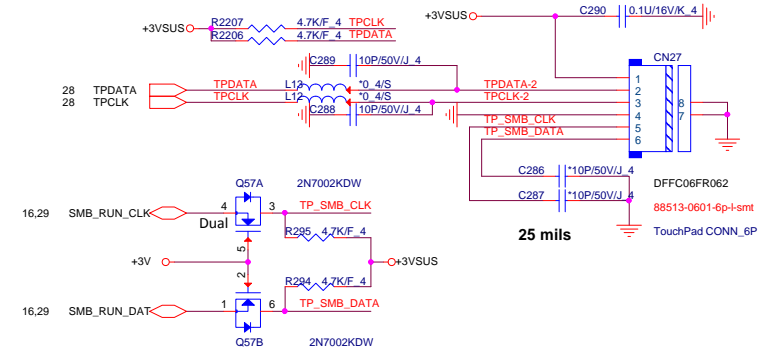


If Don't Use AMP need install

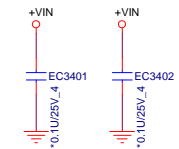
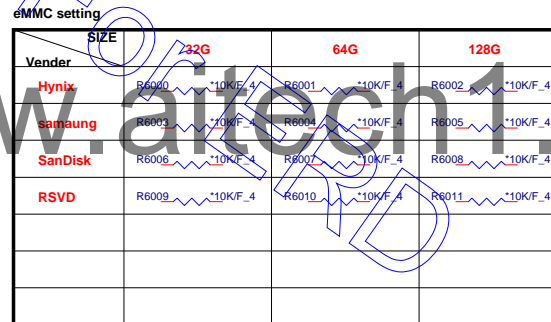












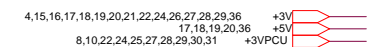
23



MEMORY TABLE



Memory setting		
SIZE	2G	4G
Hynix	R6012  *10K/F_4	R6013  *10K/F_4
samaung	R6014  *10K/F_4	R6015  *10K/F_4
Micron	R6016  *10K/F_4	R6017  *10K/F_4
RSVD	R6018  *10K/F_4	R6019  *10K/F_4

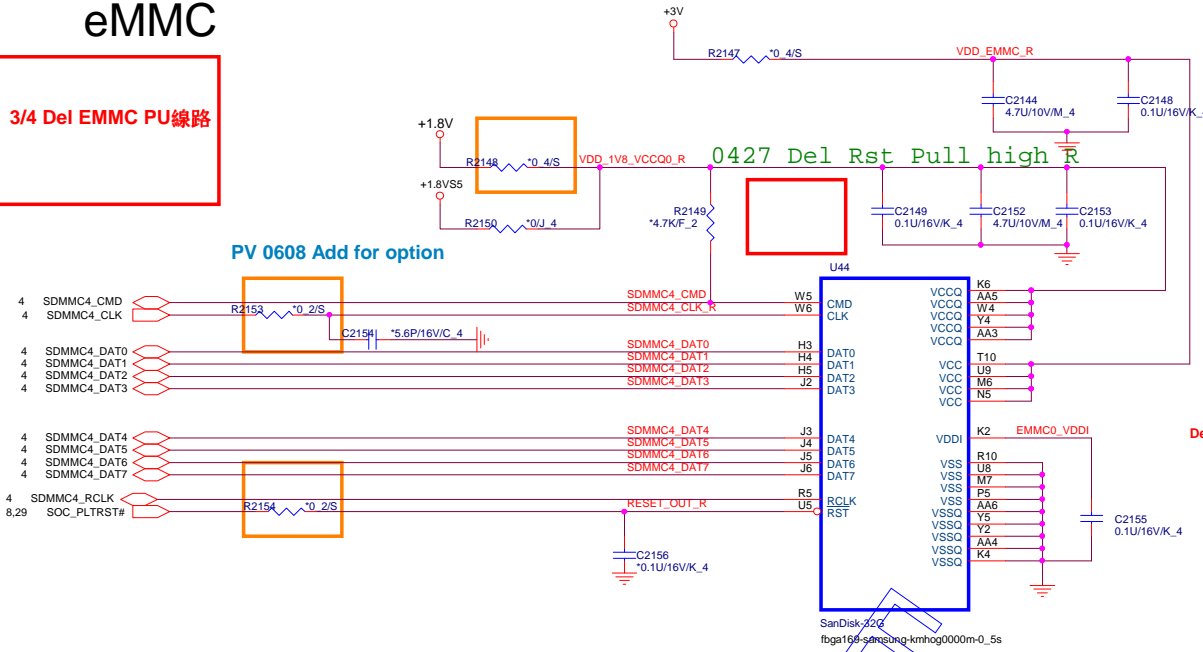


eMMC

3/4 Del EMMC PU線路

4/27 modify cap value follow FAE

PV 0608 Add for option



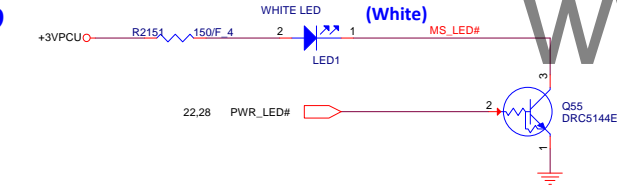
Default

iNAND (eMMC) V4.51				
TOPBSQ	QBCON	Description	SIZE	Vender
AKE3SZ-TW01	AKE3SZ-TW02	IC FLASH(153P)H26M64103EMR(FBGA)	32G	Hynix
AKE5SZ0T506	AKE5SZ0T507	IC FLASH(153P)KLMBG4GEAC-B031(BGA)	32G	samaung
AKE3SFUT000	AKE3SFUT001	IC FLASH(153P)SDIN9DW4-32G(FBGA)	32G	SanDisk
AKE3TG-TW01	AKE3TG-TW02	IC FLASH(153P)H26M78103CCR(FBGA)	64G	Hynix
AKE3TZPT515	AKE3TZPT516	IC FLASH(153P)KLMCG8GEAC-B031(BGA)	64G	samaung
AKE3TFUT101	AKE3TFUT102	IC FLASH(153P)SDIN9DW4-64G(FBGA)	64G	SanDisk

SanDisk 22G
ftga169-samsung-kmhog0000m-0_5s
footprint : BGA 169 - BGA 153 co-lay
BGA 169 PIN : 14mmX19mm
BGA 169 PIN : 12mmX18mm
BGA 153 PIN : 11.5mmX13mm

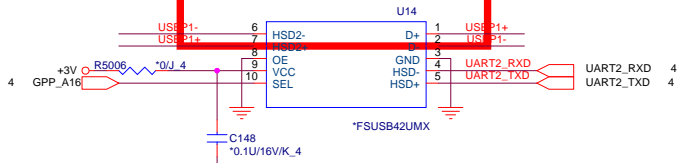
PWR LED

(White)

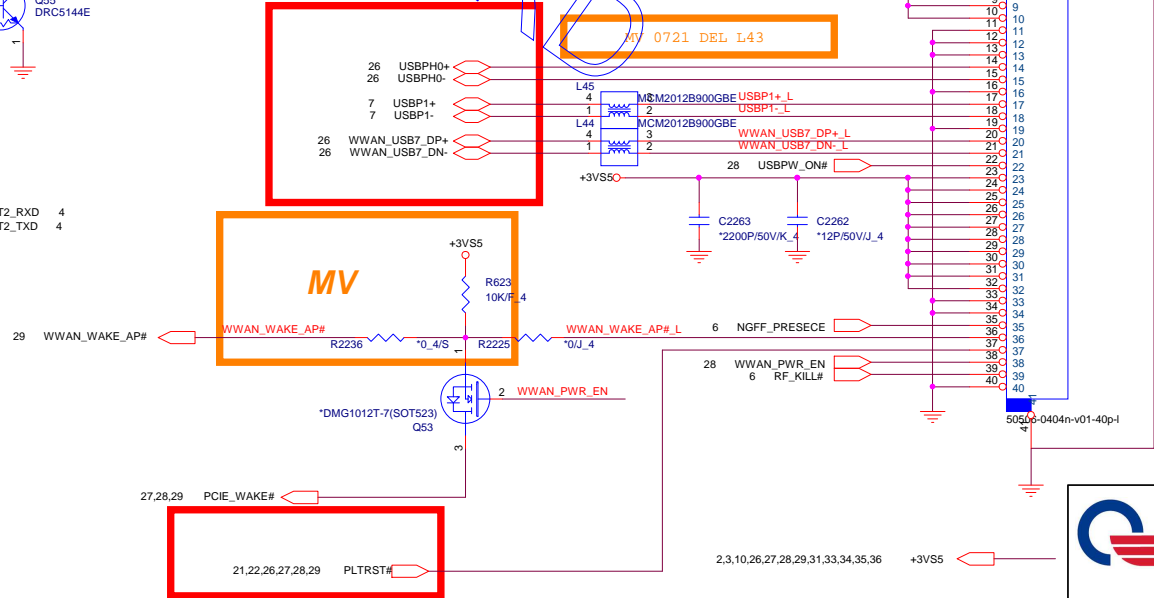


UART for DEBUG

Short USB signal / reserve footprint for debug



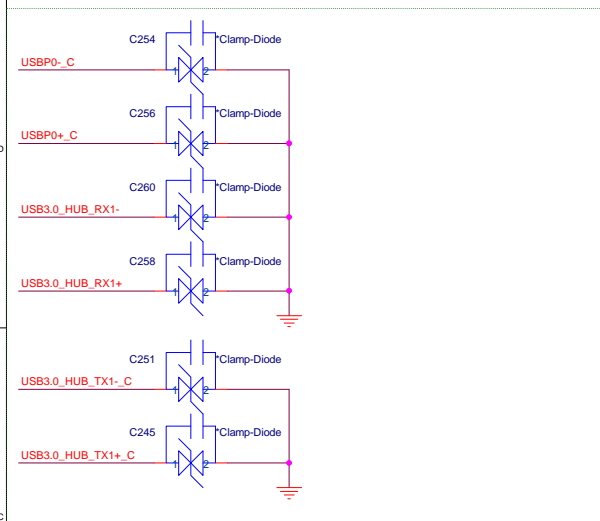
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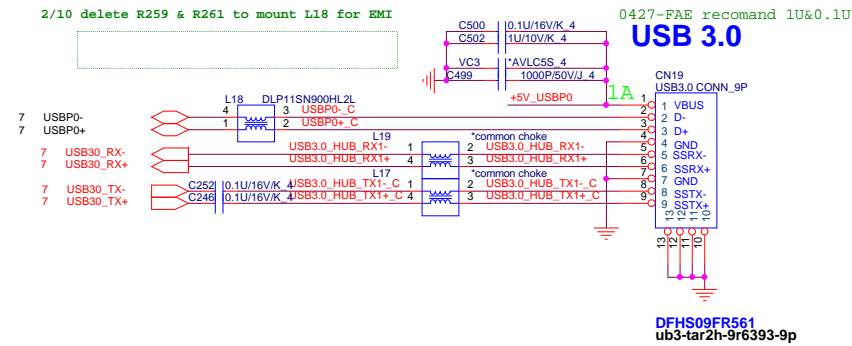
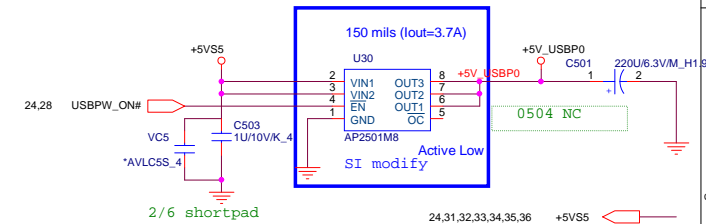
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USB 2.0/3.0 Combo

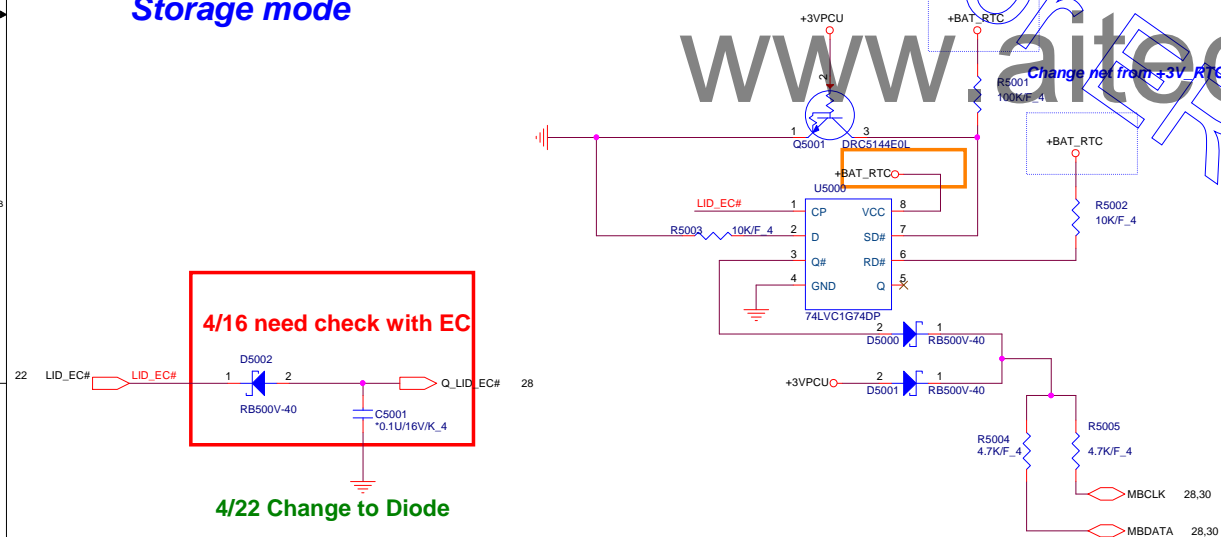


11/1 modify

2/10 delete R259 & R261 to mount L18 for EMI

DFHS09FR561
ub3-tar2h-9r6393-9p

Storage mode

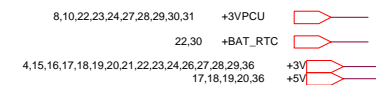


Input				Output	
SD	RD	CP	D	Q	Q̄
H	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H	H

[1] H = HIGH voltage level;
L = LOW voltage level;
X = don't care.

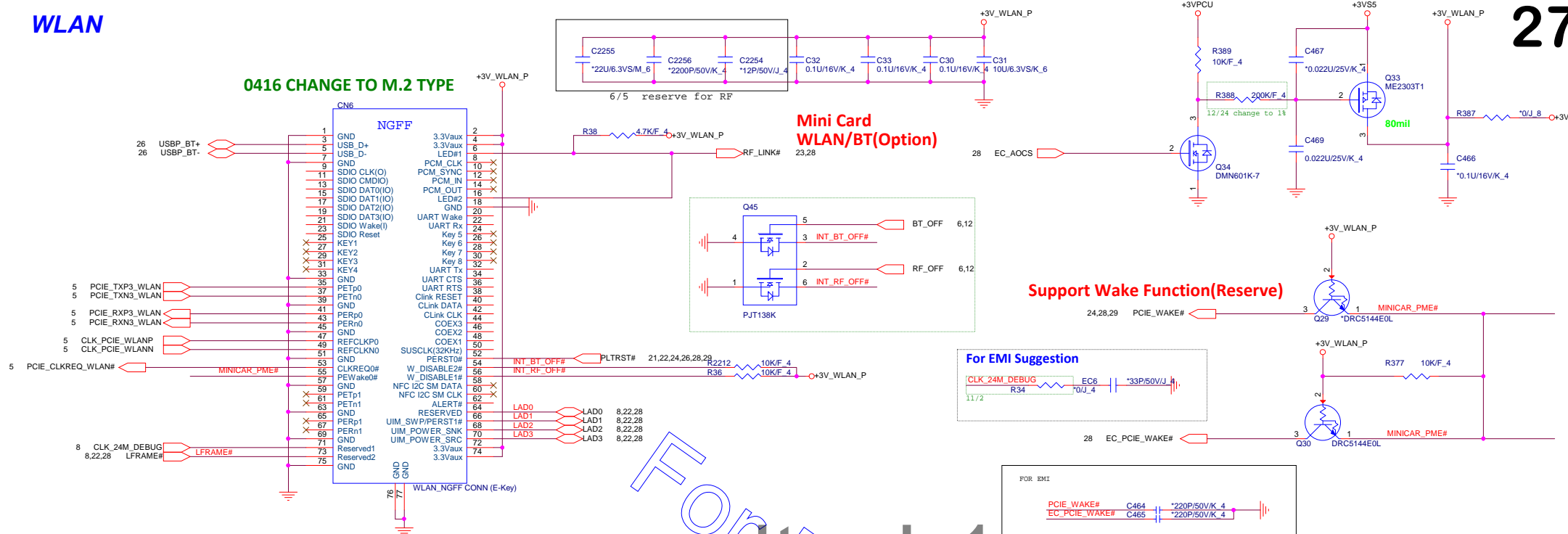
Input				Output	
SD	RD	CP	D	Q _{n+1}	Q̄ _{n+1}
H	H	↑	L	L	H
H	H	↑	H	H	L

[1] H = HIGH voltage level;
L = LOW voltage level;
↑ = LOW-to-HIGH CP transition;
Q_{n+1} = state after the next LOW-to-HIGH CP transition.

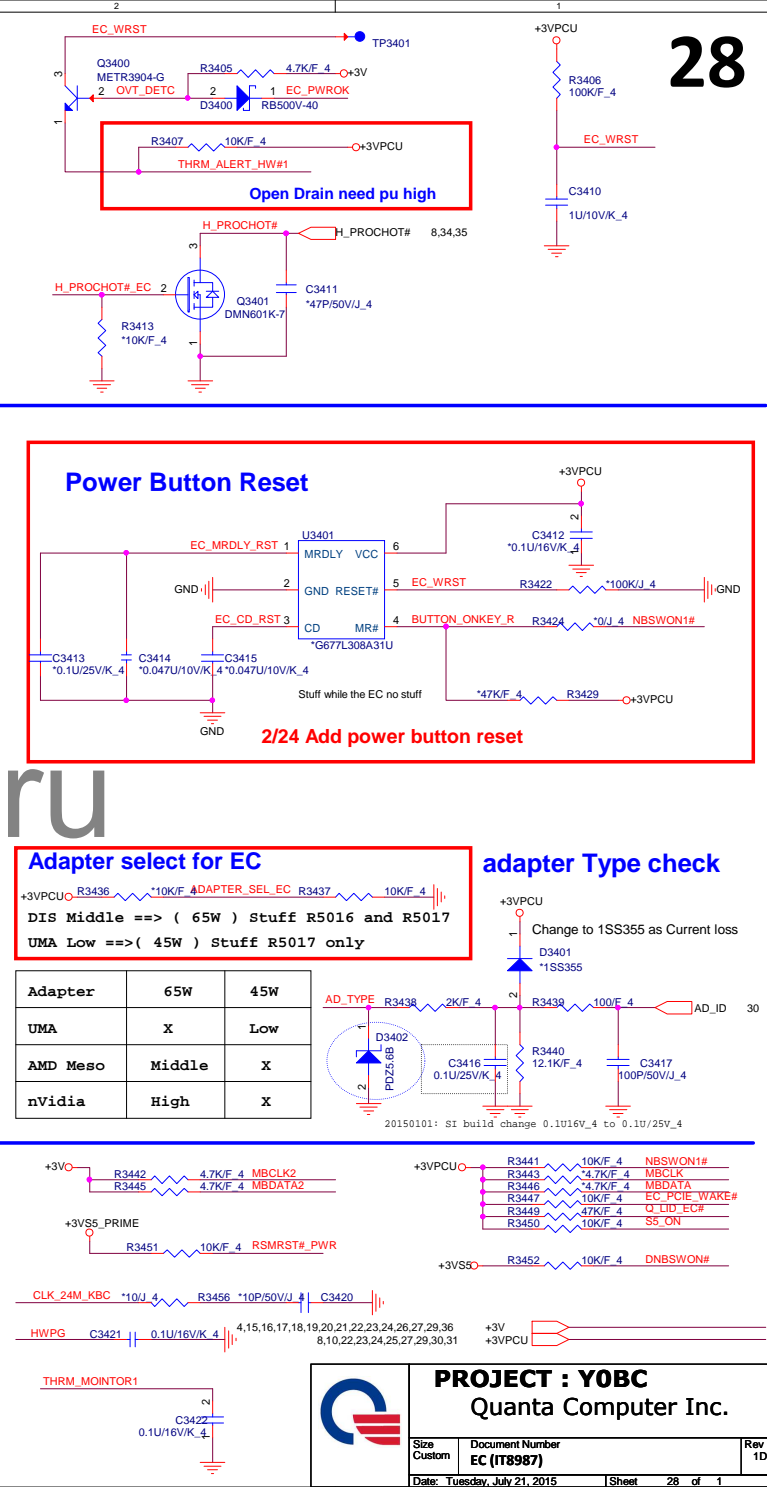
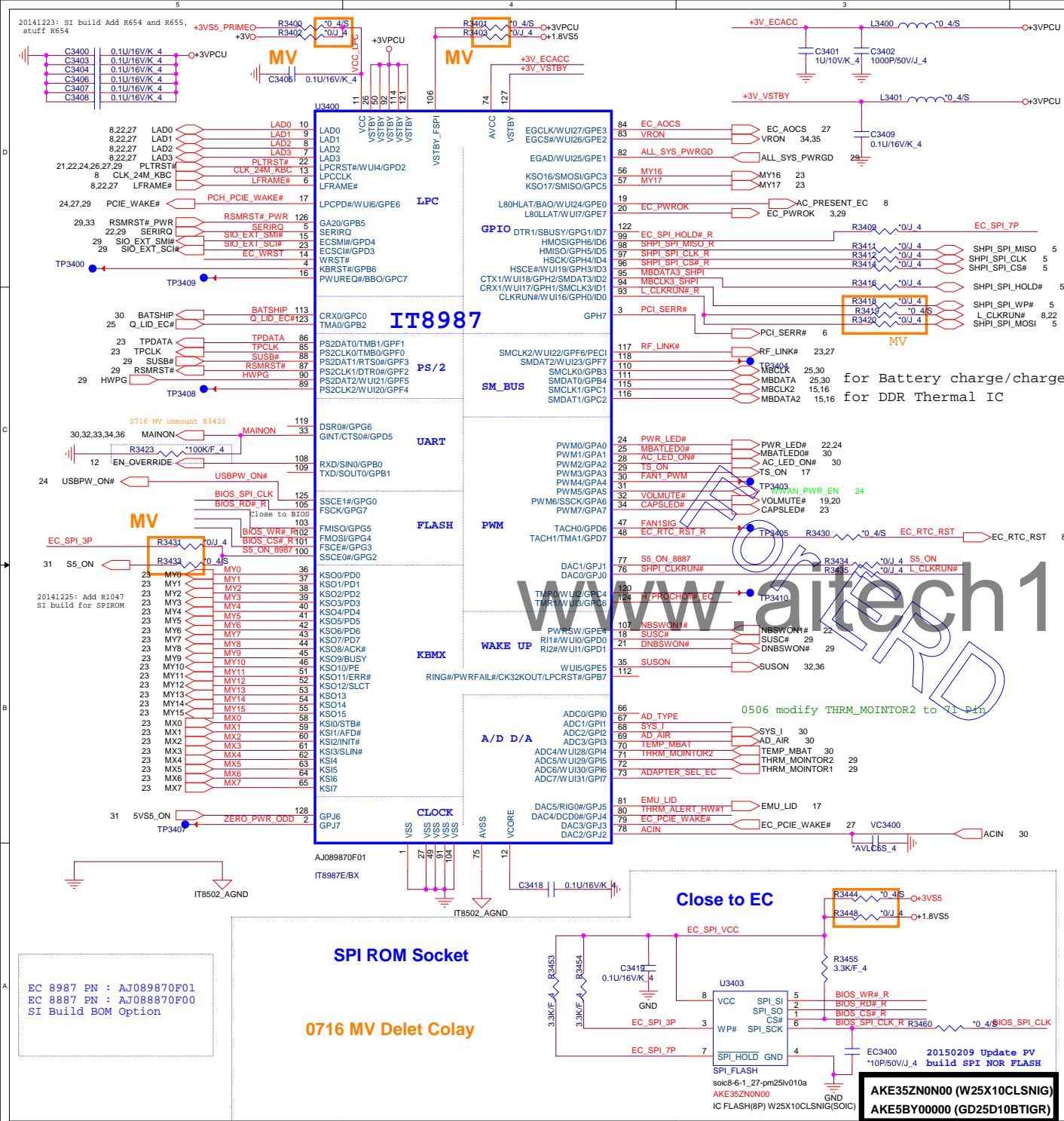


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Size	Document Number	Rev
	USB3.0/GCLK/TS/FR	1A
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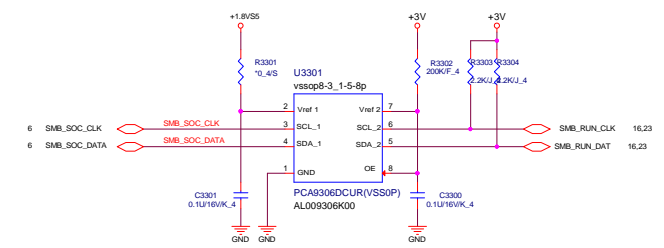
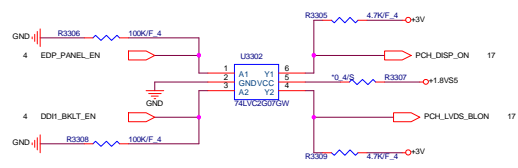
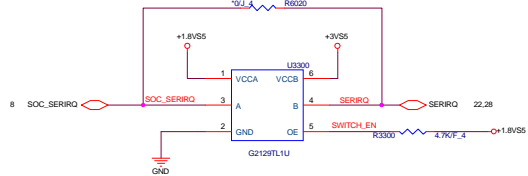
0416 CHANGE TO M.2 TYPE



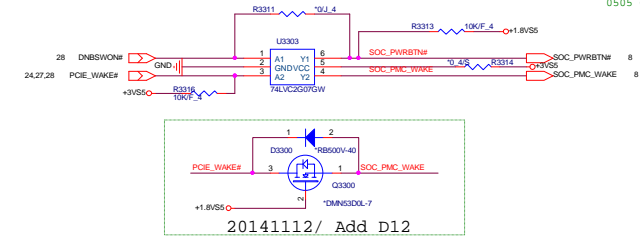
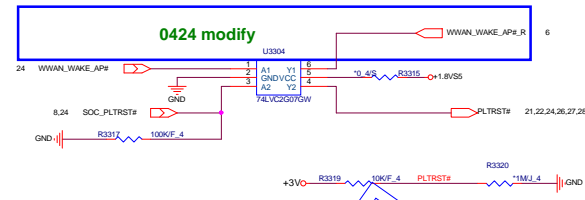
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0506 Reserve for EC



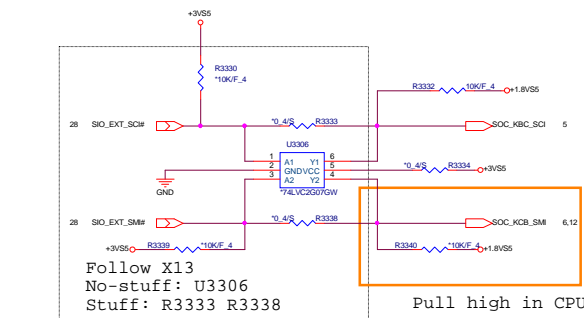
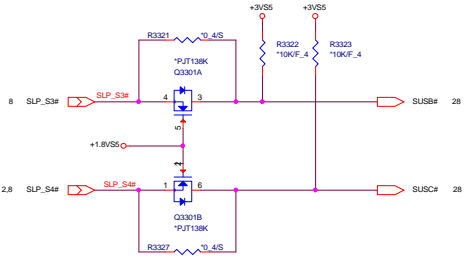
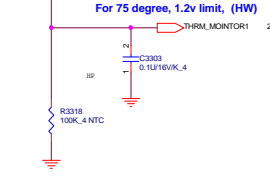
0506 NEED CHECK WITH EC AGAIN



IO Thrm Protect

For 65 degree, 1.8v limit, (SW)

For 75 degree, 1.2v limit, (HW)



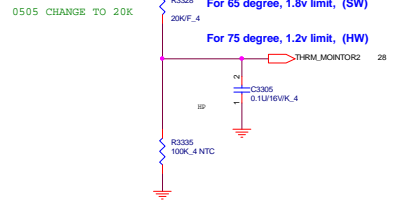
Follow X13
No-stuff: U3306
Stuff: R3333 R3338

Pull high in CPU side

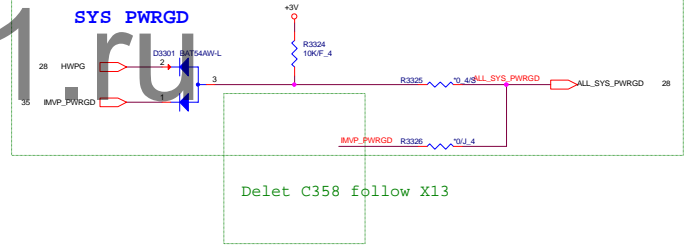
Power Thrm Protect

For 65 degree, 1.8v limit, (SW)

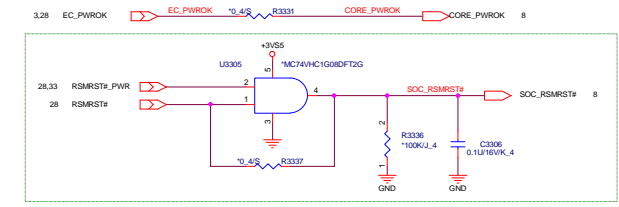
For 75 degree, 1.2v limit, (HW)



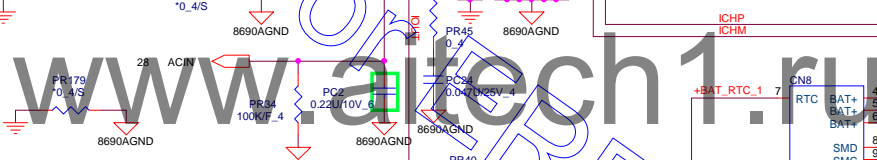
SYS PWGRD



Delet C358 follow X13

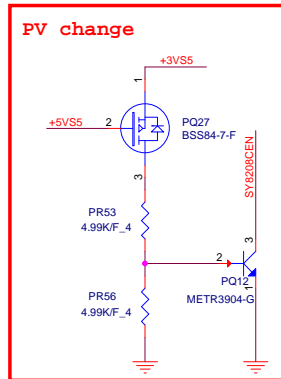


11/5 Add AND gate



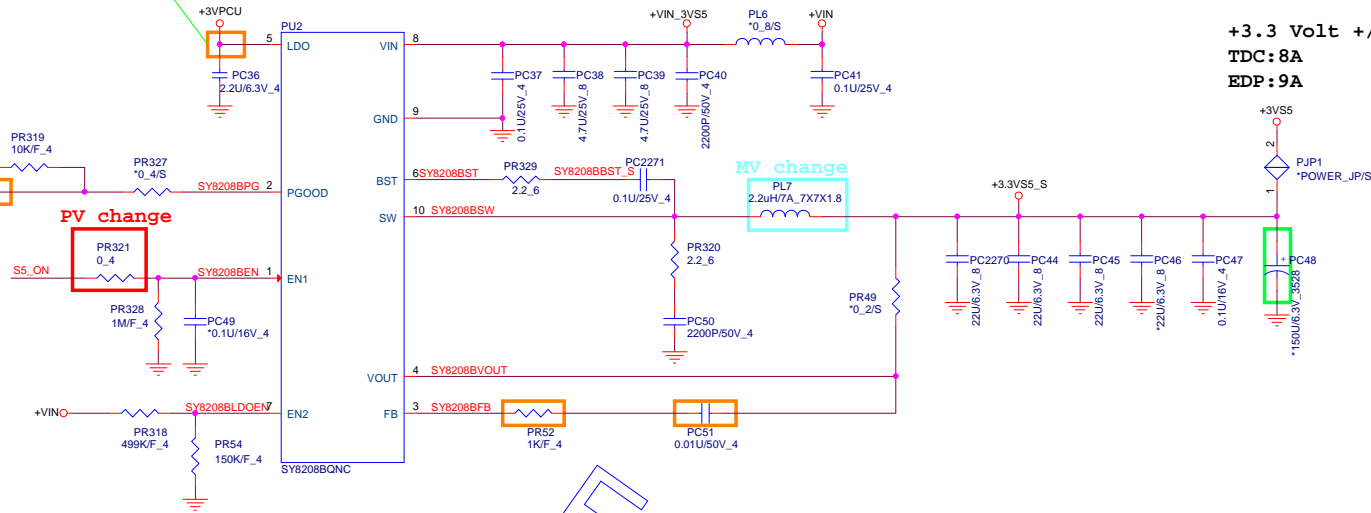
+3VS5 2,3,10,24,26,27,28,29,33,34,35,36
+5VS5 24,25,32,33,34,35,36

Do Not add test pad on VCC & LDO pin



Auto-recover PU11 latch

PV change



+3.3 Volt +/- 5%

TDC:8A

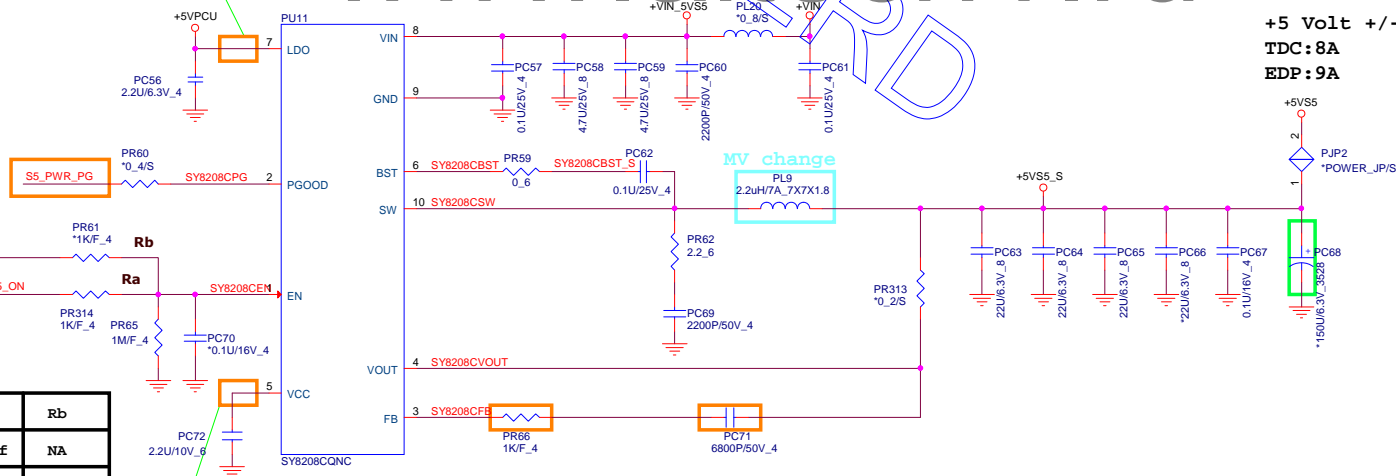
EDP:9A

Do Not add test pad on VCC & LDO pin

Reserve for USB Charge

USB Charge support	Ra	Rb
Vine (No support)	Stuff	NA
Envy (Support)	NA	Stuff

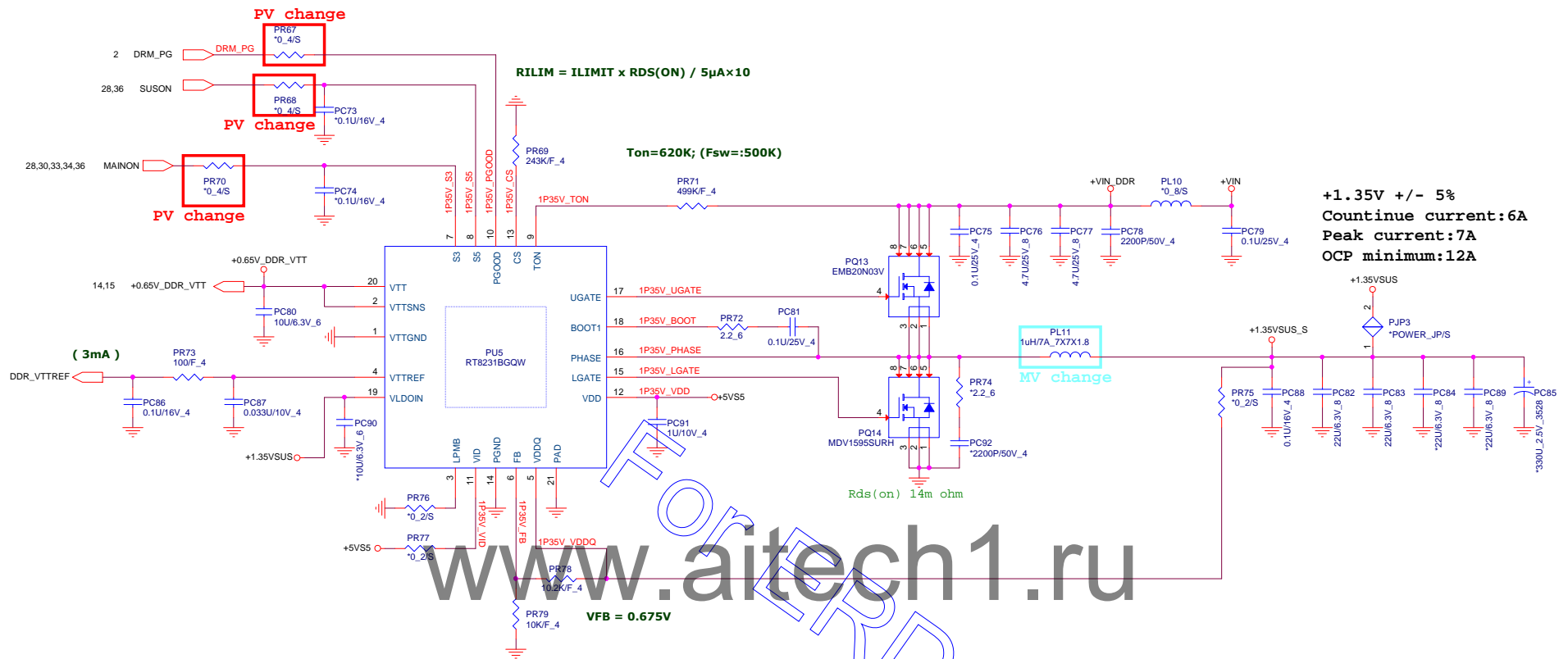
Do Not add test pad on VCC & LDO pin




+5 Volt +/- 5%

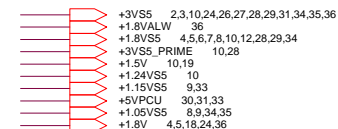
TDC:8A

EDP:9A

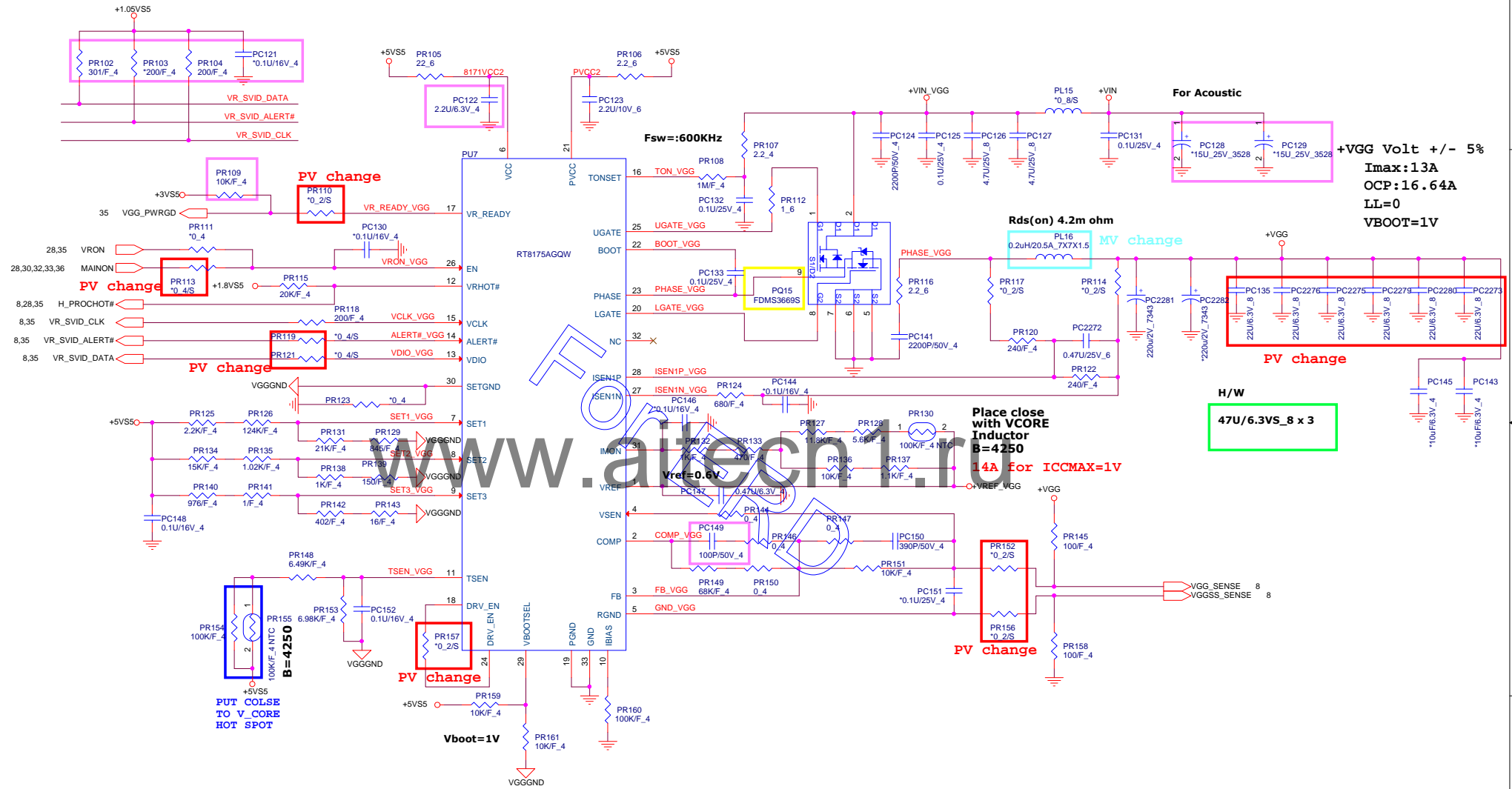


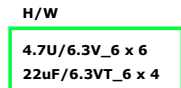
+1.35VSUS 2,3,10,14,15

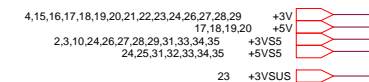
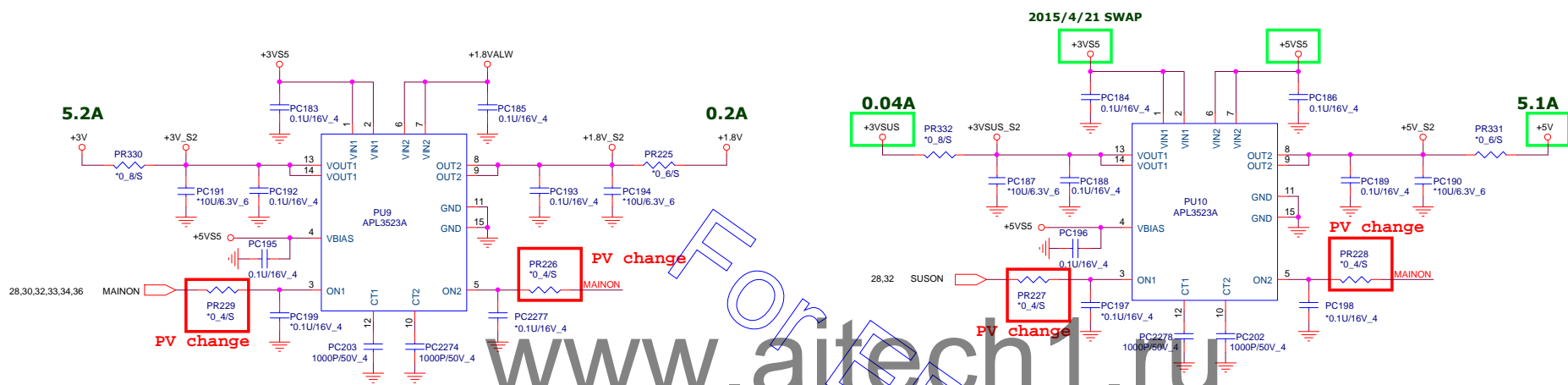
 PROJECT : YCBC Quanta Computer Inc.		
Size	Document Number DDR3 (RT8231B)1.8VS5	Rev 1A
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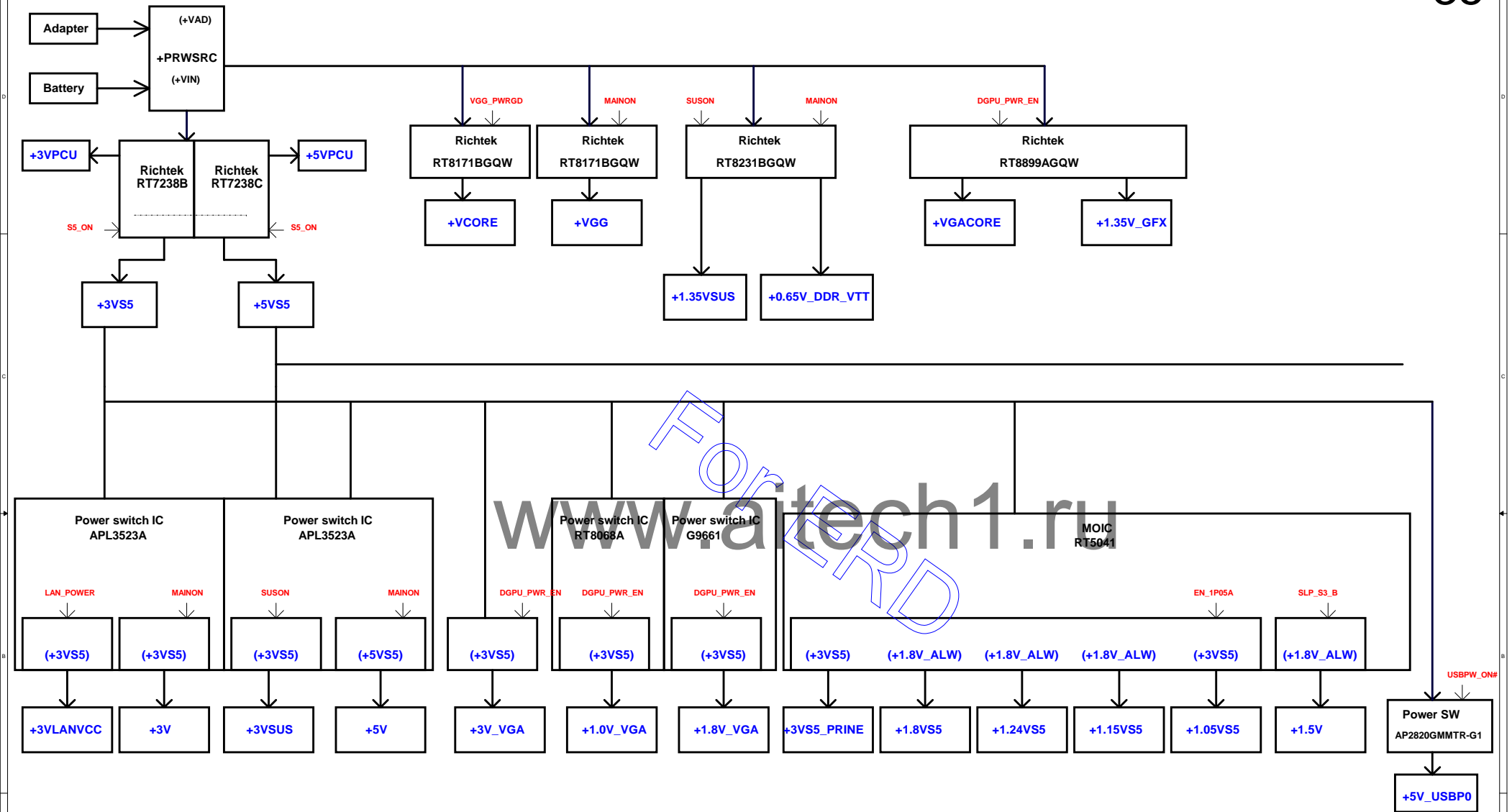
+3VS5	2,3,10,24,26,27,28,29,31,33,35,36
+1.05VS5	8,9,33,35
+5VS5	24,25,31,32,33,35,36
+VGG	9
+1.8VS5	4,5,6,7,8,10,12,28,29,33
+VIN	17,30,31,32,35

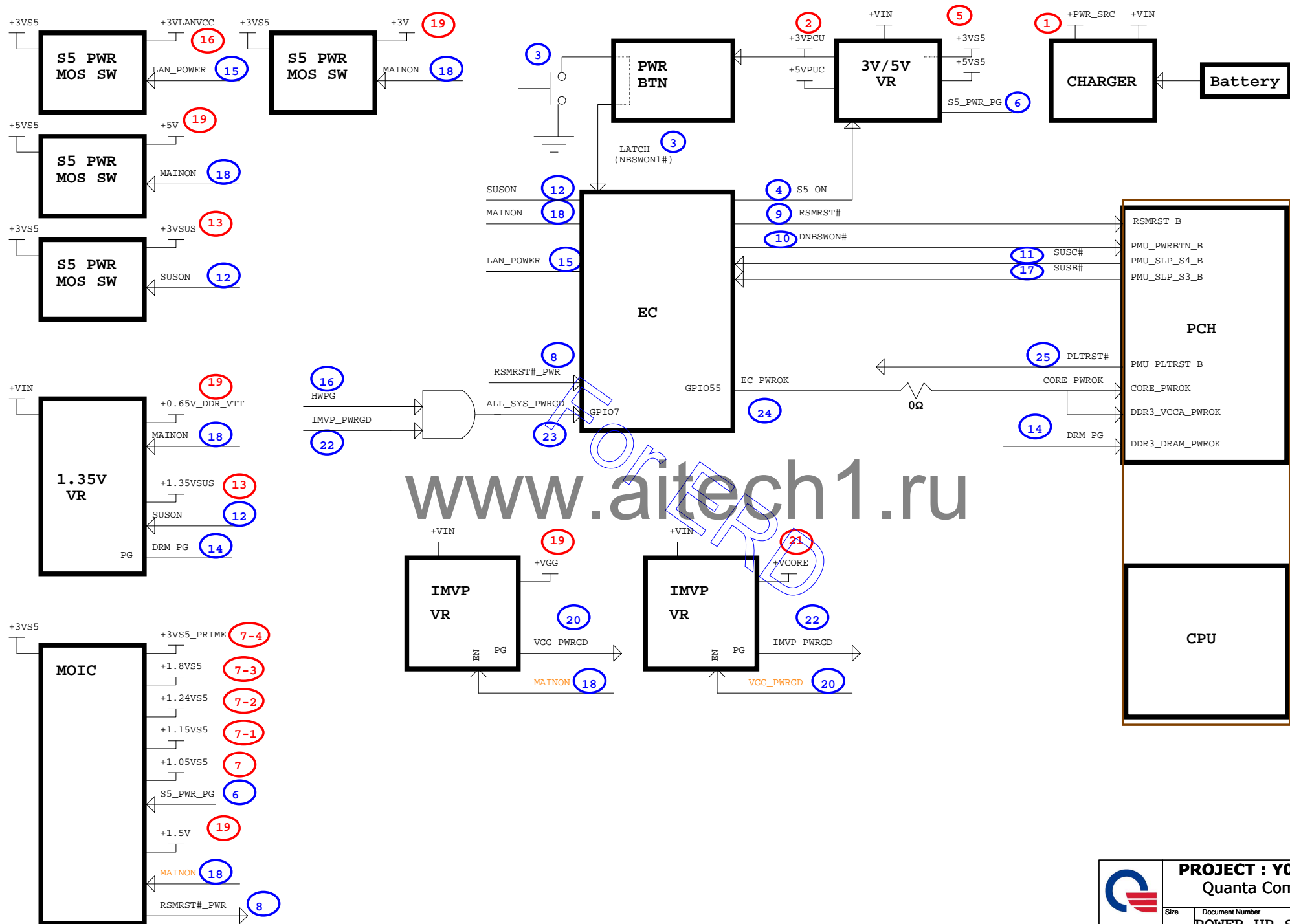


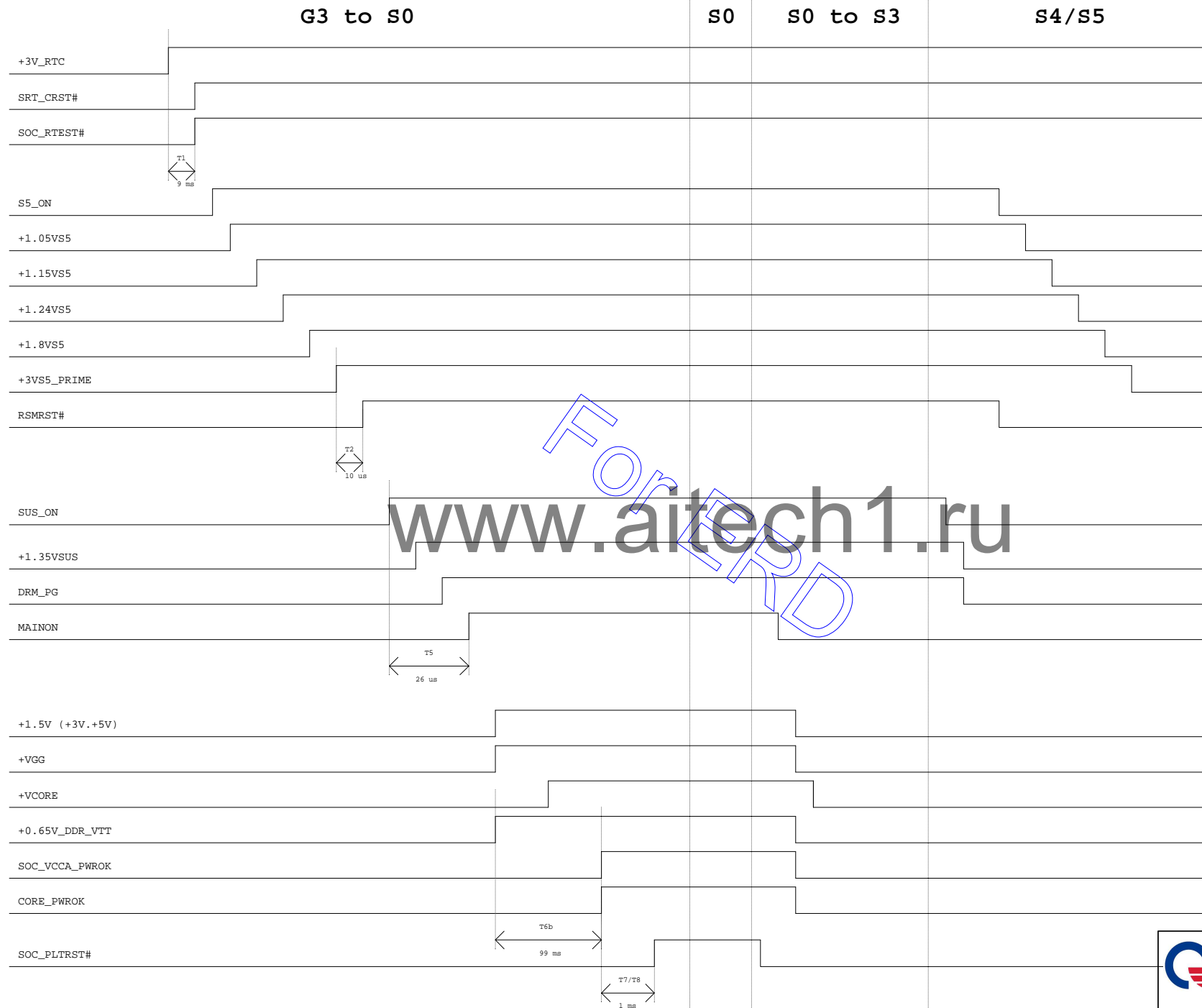




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PROJECT : Y0BC
Quanta Computer Inc.

Size	Document Number	Rev
Intel	POWER UP SEQUENCE	1A
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